What is claimed is:

1. A programmable interconnect structure for an integrated circuit comprising:

a pass-gate fabricated on a substrate layer to electrically connect a first node to a second node; and

a configuration circuit including at least one memory element to control said pass-gate fabricated substantially above said substrate layer; and

a programmable method to select between isolating said first and second nodes and connecting said first and second nodes.

2. The structure of claim 1, wherein said configuration circuit is comprised one of a thin film diode, thin film resistor, thin film capacitor and a thin film transistor.

3. The structure of claim 1, wherein said memory element is comprised one of a volatile and a non volatile memory element.

4. The structure of claim 1, wherein said memory element is selected from one of a fuse link, an anti-fuse capacitor, an SRAM cell, a DRAM cell, a metal optional link, an EPROM cell, an EEPROM cell, a flash cell, a ferro-electric element, an optical element and a magnetic element.

5. The programmable method of claim 1, further comprising:

providing a configuration access to alter data in stored memory element; and

generating a control signal from said memory element; and

controlling the polarity of said control signal by said stored memory bit polarity; and

coupling said control signal to the gate electrode of said pass-gate; and

selecting one of turning said pass gate off to isolate said first node from said second node, and turning said pass-gate on to connect said first node to second node.

6. A programmable buffer structure for an integrated circuit comprising:

a first and a second terminal; and

a programmable pull-up and a programmable pull-down circuit coupled between said first and second terminals; and

a configuration circuit including at least one memory element coupled to said pull-up and pull-down circuits; and

a programmable method to select between isolating said first terminal from second terminal by deactivating said pull-up and pull-down circuits, and coupling said first terminal to second terminal by activating said pull-up and pull-down circuits.

7. The structure of claim 6, wherein said first terminal is coupled to an output from a logic block, said logic block comprising one of fixed logic and programmable logic.

8. The structure of claim 6, wherein said second terminal is a wire comprising a capacitive load.

9. The structure of claim 6, wherein said configuration circuit is comprised of one memory element.

10. The structure of claim 6, wherein said programmable method of isolating terminals is further comprised of isolating said first and second terminals from both pull-up and pull-down circuits.

11. The structure of claim 6, wherein said programmable method of coupling is further comprised of transferring a signal at said first terminal to said second terminal by the method comprised of:

deactivating said pull-down circuit and activating said pull-up circuit to provide a source current to said second terminal; and

deactivating said pull-up circuit and activating said pull-down circuit to provide a sink current to said second terminal; and

adjusting said source and sink current strengths to provide a buffered signal at said second terminal.

12. The structure of claim 11, wherein said source current and sink current strength is adjusted by sizing said pull-up and pull-down circuit transistors respectively.

13. The structure of claim 6, further comprising a pull-up circuit comprised of:

a programmable method of selecting said first terminal and a ground voltage as the input of an inverter; and

a pull-up device controlled by output of said inverter coupled between a power supply and said second terminal.

14. The structure of claim 6, further comprising a pull-down circuit comprised of:

a programmable method of selecting said first terminal and a power voltage as the input of an inverter; and

a pull-down device controlled by output of said inverter coupled between said second terminal and a ground supply.

15. The structure of claim 6, further comprised of:

said pull-up and pull-down circuits, each comprising a pass-gate fabricated on a substrate layer; and

said configuration circuit comprising a transistor fabricated substantially above said substrate layer.

16. The structure of claim 6, wherein said configuration circuit is comprised one of a thin film diode, thin film resistor, thin film capacitor and a thin film transistor.

17. The structure of claim 6, wherein said memory element is comprised one of volatile and non volatile memory element.

18. The structure of claim 6, wherein said memory element is selected from one of a fuse link, an anti-fuse capacitor, an SRAM cell, a DRAM cell, a metal optional link, an EPROM cell, an EEPROM cell, a flash cell, a ferro-electric element, an optical element and a magnetic element.

19. The structure of claim 6, wherein said programmable method further comprises:

fabricating one or more programmable pass-gates and logic transistors on a substrate layer; and

fabricating one or more configuration access transistors and memory transistors on thin-film layers substantially above said substrate layer; and

coupling one or more control signals from said thin film memory elements to gate electrodes of said pass-gates; and

providing user access to change said thin film memory data via said thin film access transistors.

20. The method of claim 19, further comprising fabricating configuration circuits using a thin film transistor module comprising at least one of:

applying C1 mask and etching contacts;

forming W-silicide plug and performing CMP;

depositing crystalline poly-1 (P1);

performing P1 mask & etching P1;

applying blanket NMOS Vt P- implant;

applying PMOS Vt mask & N- implant;

depositing Gox;

depositing amorphous poly-2 (P2);

applying P2 mask & etching P2;

applying blanket LDN N- implant;

applying LDP mask & P- implant;

depositing a spacer oxide and etching the spacer oxide;

applying blanket N+ implantation of NMOS G/S/D;

applying P+ mask & implanting PMOS G/S/D;

depositing Nickel;

salicidizing the Nickel on the G/S/D regions & interconnect;

performing RTA anneal – P1 and P2 re-crystallization and dopant anneal;

depositing ILD oxide & CMP;

applying C2 mask & etch;

forming a W plug utilizing CMP;

depositing M1.

21. The method of claim 19, further comprising fabricating configuration circuits using a thin film transistor module comprising at least one of:

applying C1 mask and etching contacts;

forming W-silicide plug and performing CMP;

depositing crystalline poly-1 (P1);

performing P1 mask & etching P1;

applying blanket Gated-NFET Vt N- implant;

applying Gated-PFET Vt mask & P- implant;

depositing Gox;

depositing amorphous poly-2 (P2);

applying blanket P+ implantation of Gated-NFET Gate;

applying N+ mask & implanting Gated-PFET Gate;

applying P2 mask & etching P2;

applying blanket LDN N implant (Gated-NFET LDD);

applying LDP mask & P implant (Gated-PFET LDD);

depositing a spacer oxide and etching the spacer oxide;

depositing Nickel;

salicidizing the Nickel on exposed P1 and P2;

salicidizing P1 completely;

performing RTA anneal – P1 and P2 re-crystallization and dopant anneal;

depositing ILD oxide & CMP;

applying C2 mask & etch;

forming a W plug utilizing CMP;

depositing M1.

22. A bi-directional data wire structure for an integrated circuit comprising:

a wire having a first end and a second end, said wire comprising a capacitive load; and

a first programmable buffer structure, said structure as in claim 6, comprising an input and an output, said output coupled to said first end of wire; and

a second programmable buffer structure, said structure as in claim 6, comprising an input and an output, said output coupled to said second end of wire; and

a programmable method of selecting between said first buffer transmitting data and said second buffer tri-stated, and said second buffer transmitting data and said first buffer tri-stated.

23. The structure of claim 22 further comprising:

a plurality of structures, each structure as in claim 1, each coupled between said first end of wire and an external input; and

a programmable method of selecting at least one of said external inputs to connect to said wire.

24. The structure of claim 22 further comprising:

a plurality of structures, each structure as in claim 1, each coupled between said second end of wire and an external input; and

a programmable method of selecting at least one of said external inputs to connect to said wire.

25. The structure of claim 22 further comprising:

a plurality of structures, each structure as in claim 1, each coupled between said input of first programmable buffer structure and an external output; and

a programmable method of selecting at least one of said external outputs to connect to said first buffer input.

26. The structure of claim 25 further comprising:

a plurality of structures, each structure as in claim 1, each coupled between said input of second programmable buffer structure and an external output; and

a programmable method of selecting at least one of said external outputs to connect to

said second buffer input.

27. A bi-directional bus structure for an integrated circuit comprising:

a first side where said bus originates and a second side where said bus terminates; and

a plurality of bi-directional wire structures, each structure as in claim 22, each said structure further comprising:

said wire extending from said first side to said second side; and

said first buffer comprising a first side input at said first side; and

said second buffer comprising a second side input at said second side.

28. The structure in claim 27 further comprising:

a plurality of inputs, each input connecting to a first node of a plurality of interconnect structures, each structure as in claim 1, the second nodes of said plurality of structures connecting to each of said wires in said bus at said first side; and

a plurality of outputs, each output connecting to a first node of a plurality of interconnect structures, each structure as in claim 1, the second nodes of said plurality of structures connecting to each of said first side inputs of said first side buffers; and

a programmable method of selecting at least one of said inputs and one of said outputs to connect to each of said wires in said bus.

29. The structure in claim 27 further comprising:

a plurality of inputs, each input connecting to a first node of a plurality of interconnect structures, each structure as in claim 1, the second nodes of said plurality of

structures connecting to each of said wires in said bus at said second side; and

a plurality of outputs, each output connecting to a first node of a plurality of interconnect structures, each structure as in claim 1, the second nodes of said plurality of structures connecting to each of said second side inputs of said second side buffers; and

a programmable method of selecting at least one of said inputs and one of said outputs to connect to each of said wires in said bus.

30. The structure of claim 6, further comprising a pass-gate coupled between said first and second terminals, wherein:

said configuration circuit is further coupled to said pass-gate; and

said programmable method further comprises activating said pass-gate when said buffer is tri-stated, and deactivating said pass-gate when said buffer is activated.

31. The structure of claim 30, wherein said first terminal is coupled to an input/output from a logic block, said logic block comprising one of fixed logic and programmable logic.

32. The structure of claim 30, wherein said second terminal is a wire comprising a capacitive load.

33. The structure of claim 30, wherein said configuration circuit is comprised of one

memory element.

34. The structure of claim 30, wherein said programmable method comprising an activated buffer is further comprised of transferring a signal at said first terminal to said second terminal by the method comprised of:

deactivating said pull-down circuit and activating said pull-up circuit to provide a source current to said second terminal; and

deactivating said pull-up circuit and activating said pull-down circuit to provide a sink current to said second terminal; and

adjusting said source and sink current strengths to provide a buffered signal at said second terminal.

35. The structure of claim 30, further comprised of:

said pass-gate fabricated on a substrate layer; and

said pull-up and pull-down circuit comprising a pass-gate fabricated on said substrate layer; and

said configuration circuit comprising a transistor fabricated substantially above said substrate layer.

36. The structure of claim 30, wherein said configuration circuit is comprised one of a thin film diode, thin film resistor, thin film capacitor and a thin film transistor.

37. A bi-directional data wire structure for an integrated circuit comprising:

a wire having a first end and a second end, said wire comprising a capacitive load; and

a first programmable buffer structure, said structure as in claim 30, comprising an input and an output, said output coupled to said first end of wire; and

a second programmable buffer structure, said structure as in claim 30, comprising an input and an output, said output coupled to said second end of wire; and

a programmable method of selecting between said first buffer transmitting data and said second buffer receiving data, and said second buffer transmitting data and said first buffer receiving data.

38. The programmable method of claim 37, further comprising:

providing a configuration access to alter data in stored memory element; and

generating complementary control signals from said memory element; and

controlling the polarity of said control signals by said stored memory bit polarity; and

coupling said complementary control signals to said pass-gate and pull-up and pull-down circuits; and

selecting between turning said pass gate off and activating said pull-up and pull-down circuits, and turning said pass-gate on and deactivating said pull-up and pull-down circuits.

39. The structure of claim 37, further comprising:

a plurality of structures, each structure as in claim 1, each coupled between said first end of wire and an external input; and

a programmable method of selecting at least one of said external inputs to connect to said

wire.

40. The structure of claim 37, further comprising:

a plurality of structures, each structure as in claim 1, each coupled between said second end of wire and an external input; and

a programmable method of selecting at least one of said external inputs to connect to said wire.

41. The structure of claim 37, further comprising:

a plurality of structures, each structure as in claim 1, each coupled between said input of first programmable buffer structure and an external input/output; and

a programmable method of selecting at least one of said external input/outputs to connect to said first buffer input.

42. The structure of claim 37, further comprising:

a plurality of structures, each structure as in claim 1, each coupled between said input of second programmable buffer structure and an external input/output; and

a programmable method of selecting at least one of said external input/outputs to connect to said second buffer input.

43. A method of forming a programmable interconnect structure for an integrated circuit comprising:

fabricating one or more pass-gates on a substrate layer to electrically connect two

points; and

selectively fabricating either a memory circuit or a conductive pattern substantially above said pass-gates to control a portion of said pass-gates; and

fabricating an interconnect and routing layer substantially above said memory circuits to connect said pass-gates and one of said memory circuits and conductive pattern.

44. The method of claim 43, further comprised of fabricating a user configurable memory circuit on a thin film layer comprising one of fuse links, anti-fuse capacitors, SRAM, DRAM, metal optional links, EPROM, EEPROM, flash, ferro-electric, optical and magnetic memory elements.

45. The method of claim 43, further comprised of said conductive pattern comprising fabricating hard wire controls to replicate a specific memory pattern, wherein replicating comprises:

a logic zero memory output mapped to a hard wire coupled to ground; and

a logic one memory output mapped to a hard wire coupled to power.

46. The method of claim 45, wherein a given configuration of said memory circuit and the corresponding conductive pattern have one or more substantially matching signal propagation delays for said structure.

47. The method of claim 43, further comprised of said conductive pattern comprising fabricating hard wire controls to replicate a specific memory pattern, wherein replicating comprises:

a logic zero memory output mapped to a hard wire coupled to ground; and

a logic one memory output mapped to a hard wire shorting drain to source of pass-gate controlled by said logic one memory element.

48. The method of claim 47, wherein a given configuration of said memory circuit operated at an elevated memory power supply voltage and the corresponding conductive pattern have one or more substantially matching signal propagation delays for said switch.